Features:

- ✧ 4 CWDM lanes MUX/DEMUX design
- ✧ Up to 11.2Gbps per channel bandwidth
- ✧ Aggregate bandwidth of > 40Gbps
- ✧ Duplex LC connector
- ✧ Compliant with 40G Ethernet IEEE802.3ba and 40GBASE-ER4 Standard
- ✧ QSFP MSA compliant
- ✧ Up to 40km transmission
- ✧ Compliant with QDR/DDR Infiniband data rates
- ✧ Single +3.3V power supply operating
- ✧ Built-in digital diagnostic functions
- ✧ Temperature range 0°C to 70°C
- ✧ RoHS Compliant

Applications

- ✧ Rack to rack
- ✧ Data centers Switches and Routers
- ✧ Metro networks
- ✧ Switches and Routers
- ✧ 40G BASE-ER4 Ethernet Links

Description:

The OPQC40 is a transceiver module designed for 40Km optical communication applications. The design is compliant to 40GBASE-ER4 of the IEEE P802.3ba standard. The module converts 4 inputs channels(ch) of 10Gb/s electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 40Gb/s input into 4 CWDM channels signals, and converts them to 4 channel output electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G694.2. It contains a duplex LC connector for the optical interface and a 38-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

The module operates from a single +3.3V power supply and LVCMOS/LVTTL global control signals such as Module Present, Reset, Interrupt and Low Power Mode are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals and to obtain digital diagnostic information. Individual channels can be addressed and unused channels

can be shut down for maximum design flexibility.

This product converts the 4-channel 10Gb/s electrical input data into CWDM optical signals (light), by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX parts as a 40Gb/s data, propagating out of the transmitter module from the SMF. The receiver module accepts the 40Gb/s CWDM optical signals input, and de-multiplexes it into 4 individual 10Gb/s channels with different wavelength. Each wavelength light is collected by a discrete avalanche photodiode (APD), and then outputted as electric data after amplified first by a TIA and then by a post amplifier.

The OPQC40 is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

● Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	T_S	-40		+85	℃
Supply Voltage	$V_{CC}T$, R	-0.5		4	V
Relative Humidity	RH	0		85	%

● Recommended Operating Environment:

Parameter	Symbol	Min.	Typical	Max.	Unit
Case operating Temperature	T_C	0		+70	℃
Supply Voltage	$V_{CCT, R}$	+3.13	3.3	+3.47	V
Supply Current	I_{CC}			1100	mA
Power Dissipation	PD			3.5	W

● Electrical Characteristics (T_{OP} = 0 to 70 °C, VCC = 3.135 to 3.465 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data Rate per Channel		-	10.3125	11.2	Gbps	
Power Consumption		-	2.5	3.5	W	
Supply Current	Icc		0.75	1.1	A	
Control I/O Voltage-High	VIH	2.0		Vcc	V	
Control I/O Voltage-Low	VIL	0		0.7	V	
Inter-Channel Skew	TSK			150	Ps	
RESETL Duration			10		Us	
RESETL De-assert time				2000	ms	
Power On Time				2000	ms	
Transmitter						
Single Ended Output Voltage Tolerance		0.3		4	V	1

Common mode Voltage Tolerance		15			mV	
Transmit Input Diff Voltage	VI	150		1200	mV	
Transmit Input Diff Impedance	ZIN	85	100	115		
Data Dependent Input Jitter	DDJ		0.3		UI	
Receiver						
Single Ended Output Voltage Tolerance		0.3		4	V	
Rx Output Diff Voltage	Vo	370	600	950	mV	
Rx Output Rise and Fall Voltage	Tr/Tf			35	ps	1
Total Jitter	TJ		0.3		UI	

Note:

1. 20～80%

● Optical Characteristics (T_{OP} = 0 to 70°C, VCC = 3.135 to 3.465 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Wavelength Assignment	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Side-mode Suppression Ratio	SMSR	30	-	-	dB	
Total Average Launch Power	PT	-	-	+10.5	dBm	
Average Launch Power, each Lane		-2.7	-	+4.5	dBm	
Difference in Launch Power between any two Lanes (OMA)		-	-	6.5	dB	
Optical Modulation Amplitude, each Lane	OMA	-0.7		+5	dBm	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-1.5	-		dBm	
TDP, each Lane	TDP			2.6	dB	
Extinction Ratio	ER	5.5	-	-	dB	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Optical Return Loss Tolerance		-	-	20	dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Relative Intensity Noise	Rin			-128	dB/HZ	1
Receiver						
Damage Threshold	THd	3.8			dBm	1

Average Power at Receiver Input, each Lane	R	-21.2		-4.5	dBm	
Receiver Power (OMA), each Lane				-1	dB	
RSSI Accuracy		-2		2	dB	
Receiver Reflectance	Rrx			-26	dB	
Stressed Receiver Sensitivity in OMA, each Lane		-	-	-16.8	dBm	
Receiver Sensitivity(OMA), each Lane	Sen	-	-	-19	dBm	
Difference in Receive Power between any two Lanes (OMA)				7.5	dB	
Receive Electrical 3 dB upper Cutoff Frequency, each Lane				12.3	GHz	
LOS De-Assert	LOS_D			-22	dBm	
LOS Assert	LOS_A	-35			dBm	
LOS Hysteresis	LOS_H	0.5			dB	

Note:

1. 12dB Reflection

● Diagnostic Monitoring Interface

Digital diagnostics monitoring function is available on all QSFP+ LR4. A 2-wire serial interface provides user to contact with module. The structure of the memory is shown in flowing. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

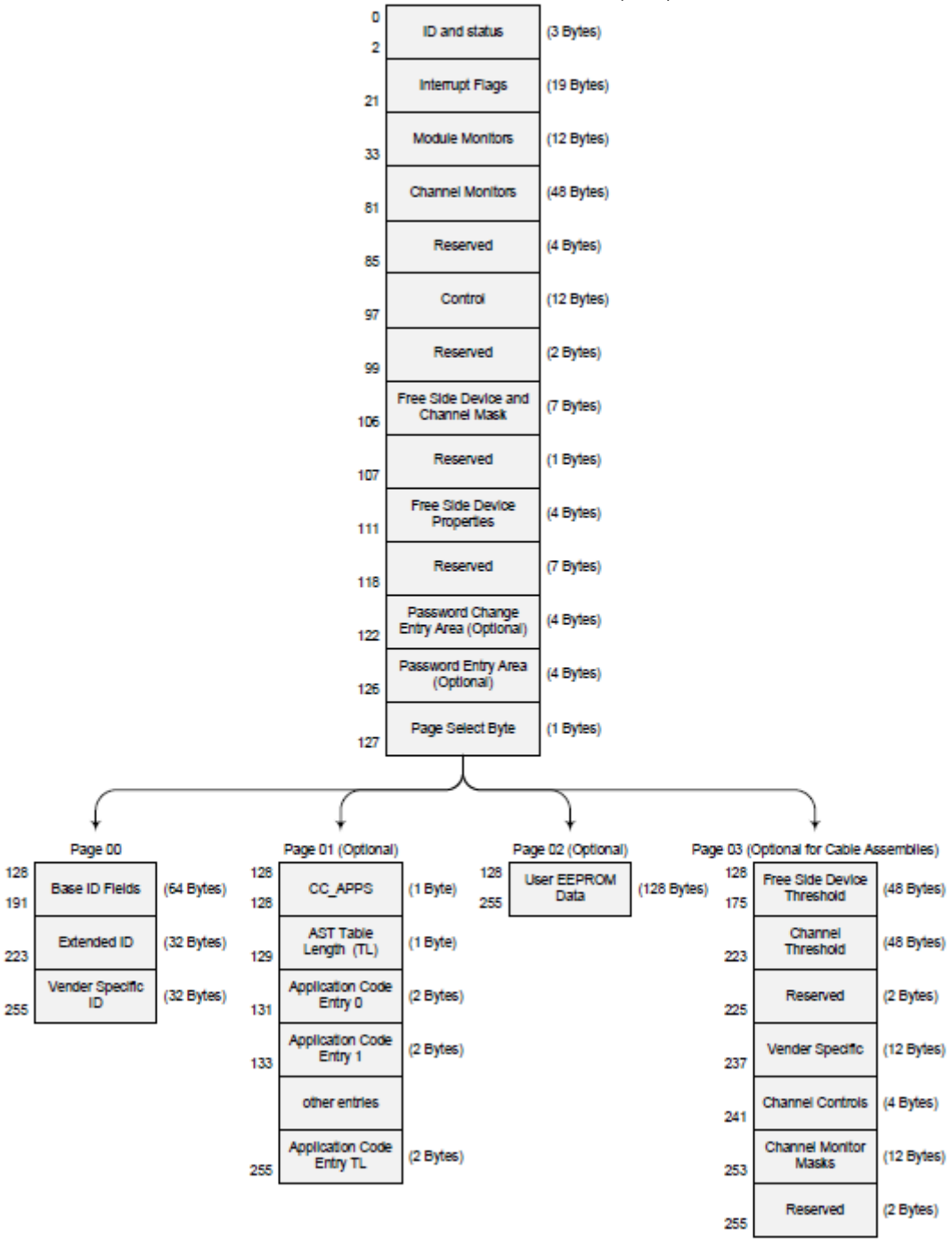
Lower Memory Map (A0h)

Address	Size (Bytes)	Description	Type
0	1	Identifier	Read-Only
1-2	2	Status	Read-Only
3-21	19	Interrupt Flags	Read-Only
22-33	12	Module Monitors	Read-Only
34-81	48	Channel Monitors	Read-Only
82-85	4	Reserved	Read-Only
86-97	12	Control	Read/Write
98-99	2	Reserved	Read/Write
100-106	7	Module and Channel Masks	Read/Write
107-118	12	Reserved	Read/Write
119-122	4	Reserved	Read/Write
123-126	4	Reserved	Read/Write
127	1	Page Select Byte	Read/Write

Upper Memory Map Page 03h

Address	Size (Bytes)	Description	Type
128-175	48	Module Thresholds	Read-Only
176-223	48	Reserved	Read-Only
224-225	2	Reserved	Read-Only
226-239	14	Reserved	Read/Write
240-241	2	Channel Controls	Read/Write
242-253	12	Reserved	Read/Write
254-255	2	Reserved	Read/Write

2-Wire Serial Address: 1010000x (A0h)



QSFP Memory Map

Serial ID: Data Fields

Address	Size (Bytes)	Name	Description of Base ID Field
Base ID fields			
128	1	Identifier	Identifier Type of serial Module
129	1	Ext. Identifier	Extended Identifier of Serial Module
130	1	Connector	Code for connector type
131-138	8	Specification compliance	Code for electronic compatibility or optical compatibility
139	1	Encoding	Code for serial encoding algorithm
140	1	BR, nominal	Nominal bit rate, units of 100 MBits/s
141	1	Extended Rate select Compliance	Tags for extended rate select compliance
142	1	Length(SMF)	Link length supported for SMF fiber in km
143	1	Length(OM3 50um)	Link length supported for EBW 50/125um fiber (OM3), units of 2m
144	1	Length(OM2 50um)	Link length supported for 50/125um fiber (OM2), units of 1m
145	1	Length(OM1 62.5 um)	Link length supported for 62.5/125um fiber (OM1), units of 1m
146	1	Length (Copper)	Link length of copper or active cable, units of 1m
147	1	Device tech	Device technology
148-163	16	Vendor name	QSFP+ vendor name(ASCII)
164	1	Extended Module	Extended Module codes for InfiniBand
165-167	3	Vendor OUI	QSFP+ vendor IEEE company ID
168-183	16	Vendor PN	Part number provided by QSFP+ vendor(ASCII)
184-185	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
186-187	2	Wave length or Copper Cable Attenuation	Nominal laser wavelength (wavelength=value/20 in nm)
188-189	2	Wavelength tolerance	Guaranteed range of laser wavelength(+/- value) from nominal wavelength. (wavelength Tol.=value/200 in nm)
190	1	Max case temp.	Maximum case temperature in degrees C
191	1	CC_BASE	Check code for base ID fields (addresses 128-190)
Extended ID fields			
192-195	4	Options	Rate Select, TX Disable, TX Fault, LOS
196-211	16	Vendor SN	Serial number provided by vendor (ASCII)
212-219	8	Date Code	Vendor’s manufacturing date code
220	1	Diagnostic Monitoring Type	Indicates which types of diagnostic monitoring are implemented (if any) in the Module. Bit 1,0 Reserved
221	1	Enhanced Options	Indicates which optional enhanced features are implemented in the transceiver.
222	1	Reserved	
223	1	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
Vendor Specific ID Fields			
224-255	32	Vendor Specific EEPROM	

Page02 is User EEPROM and its format decided by user.
The detail description of low memory and page00.page03 upper memory please see SFF-8436 document.

● Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on1, hot plug or rising edge of Reset

				until the module is fully functional2
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional2
LPMode Assert Time	ton_LPMode	100	μs	Time from assertion of LPMode (Vin:LPMode =Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	toff_IntL 500 μs Time from clear on read3 operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set4 until associated IntL assertion is inhibited
Mask De-assert Time	toff_mask	100	ms	Time from mask bit cleared4 until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set 4 until module power consumption enters lower Power Level
Power_over-ride or Power-set De-assert Time	toff_Pdown	300	ms	Time from P_Down bit cleared4 until the module is fully functional3

Note:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

Transceiver Block Diagram

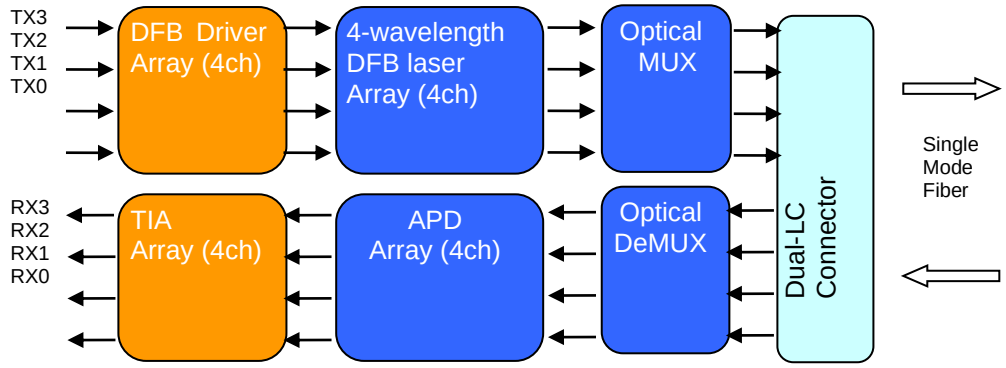
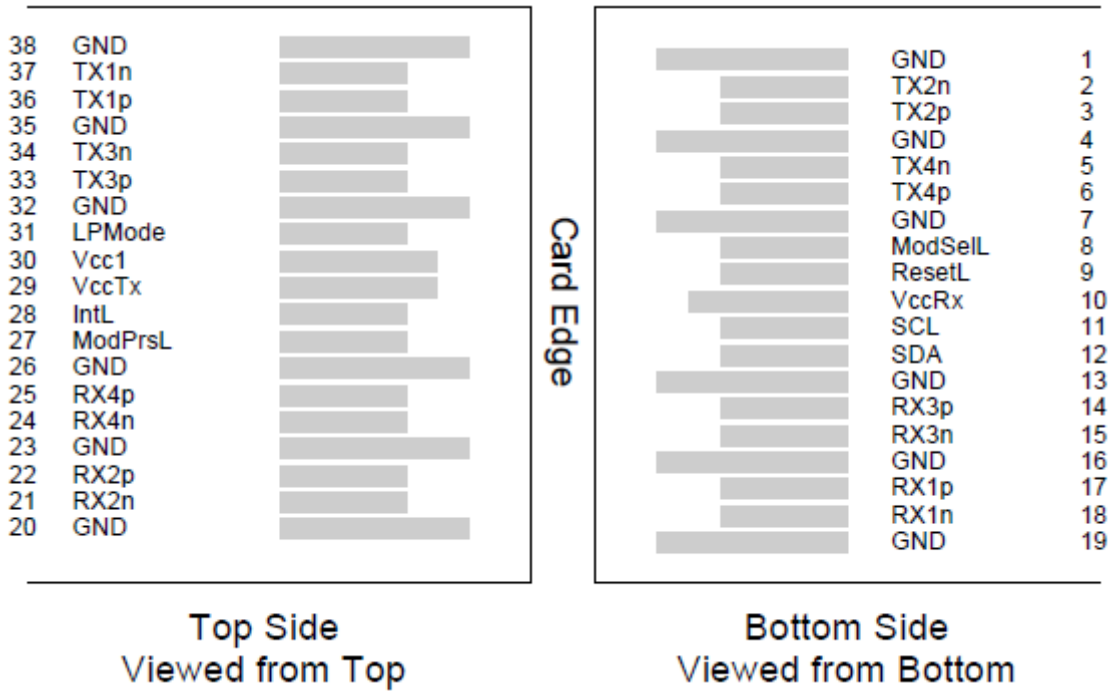


Figure 1: 40Gb/s QSFP ER4 Transceiver Block Diagram

Pin Assignment:



QSFP Transceiver Pad Layout

Pin Function Definitions

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	

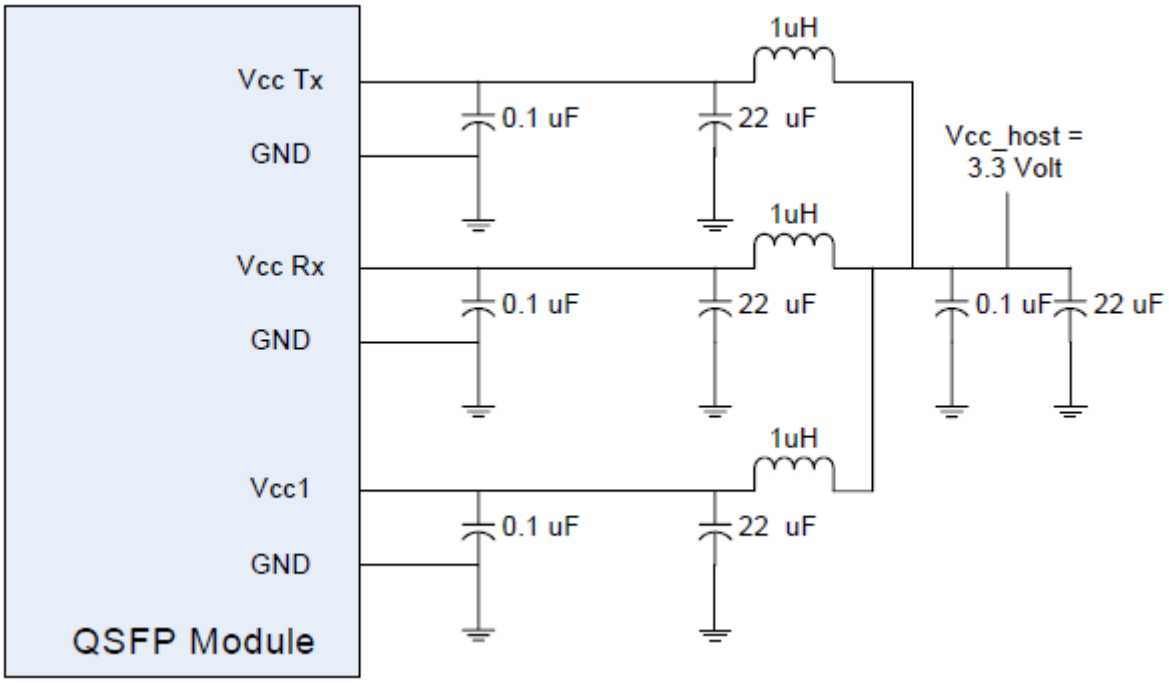
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Inverted Data Output	
15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

Notes:

1.GND is the symbol for single and supply(power) common for QSFP modules, All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.

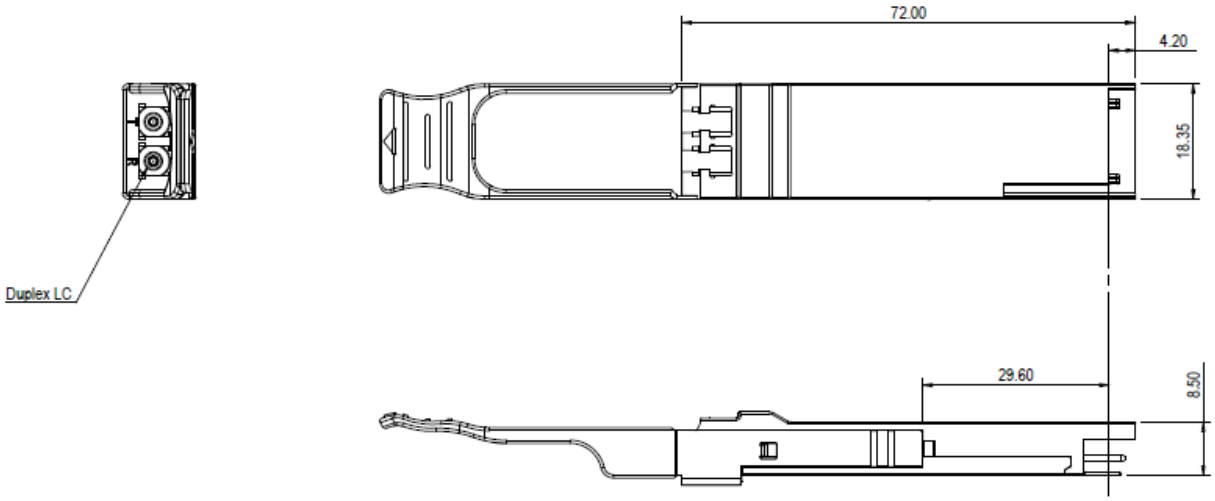
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for maximum current of 500mA.

Recommended Circuit:



Recommended Host Board Power Supply Filtering

Mechanical Dimensions:



Published by Shenzhen OPWAY Communication Co., Ltd.

Shenzhen Opway Communication Co., Ltd.
3F, Building 5, Section 2, Baiwangxin High-tech Industrial Park,1002 Songbai Rd., Nanshan, Shenzhen ,Guangdong,China 518000
Tel: +86-755-86000306 Fax: +86-755-86000825
E-mail: info@opwaytech.com http://www.opwaytech.com