FEATURES

1.Compliant with IEEE 802.3bs standard:
  -200GBASE-LR8 optical interface
  -200GAUI-8 electrical interface
2.Compliant with QSFP-DD MSA HW Rev 5.0 with duplex LC connector
3.Compliant with QSFP-DD CMIS Rev 4.0
4.Case operating temperature 0°C to 70°C
5.Two wire serial Interface with digital diagnostic monitoring
6.RoHS compliant
7.Class 1 Laser

Description

The Opway's OPDH10 is an Eight-Channel, Pluggable, Fiber-Optic QSFP DD LR8 for 200G Ethernet applications. This transceiver is a high performance module for data communication and interconnect applications. It integrates eight data lanes in each direction with 206.25Gbps bandwidth. Each lane can operate at 25.78125Gbps up to 10km over G.652 SMF. These modules are designed to operate over single-mode fiber systems using 8 LAN-WDM wavelengths. The electrical interface uses a 76 contact edge type connector. The optical interface uses duplex LC connector.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
OperatingCase Temperature	T_c	0		70	ºC
Data Rate Per Lane	fd		25.78125		Gbps
Humidity	Rh	5		85	%
Power Dissipation	P_m			7.5	W
Fiber Bend Radius	R_b	0.002		10	km

Shenzhen Opway Communication Co., Ltd.
3F, Building 5, Section 2, Baiwangxin High-tech Industrial Park,1002 Songbai Rd., Nanshan, Shenzhen ,Guangdong,China 518000
Tel: +86-755-86000306 Fax: +86-755-86000825
E-mail: info@opwaytech.com http://www.opwaytech.com

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude[1]	ΔV_{in}	190		700	mVp-p
Differential Output Voltage Amplitude[2]	ΔV_{out}	300		850	mVp-p
Input Logic Level High	V_{IH}	2.0		V_{cc}	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	V_{cc}-0.5		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V

Note:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

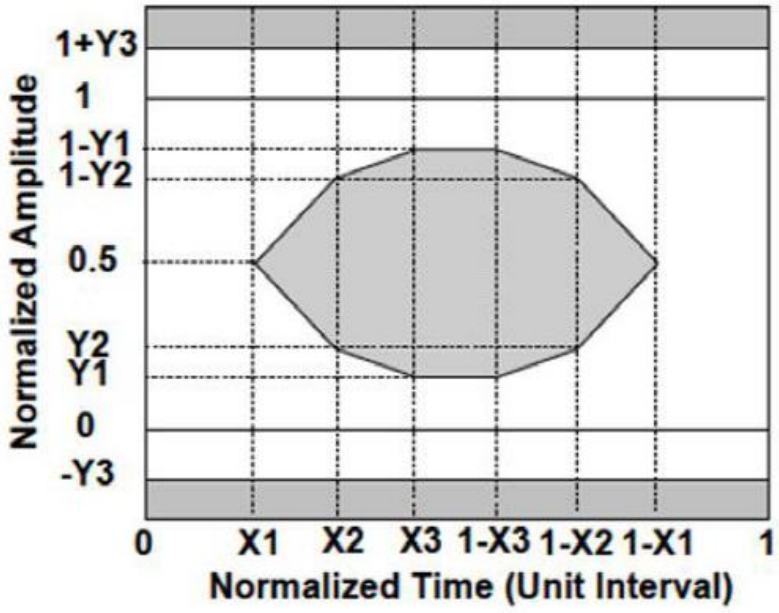
200GBASE-LR8						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Lane Wavelength	L0	1272.55	1273.54	1274.54	nm	
	L1	1276.89	1277.89	1278.89	nm	
	L2	1281.25	1282.26	1283.27	nm	
	L3	1285.65	1286.66	1287.68	nm	
	L4	1294.53	1295.56	1296.59	nm	
	L5	1299.02	1300.05	1301.09	nm	
	L6	1303.54	1304.58	1305.63	nm	
	L7	1308.09	1309.14	1310.19	nm	
Transmitter						
SMSR	SMSR	30			dB	
Total Average Launch Power	P_T			10.5	dBm	
Average Launch Power, each Lane	P_{AVG}	-3.4		5.3	dBm	
OMA, each Lane	P_{OMA}	-1.3		5.3	dBm	1
Difference in Launch Power	Ptx,diff			5	dB	
Launch Power in OMA		-2.3			dBm	
TDP, each Lane	TDP			2.2	dB	
Extinction Ratio	ER	4			dB	

$RIN_{20}OMA$	RIN			-130	dB/H	
Optical Return Loss	TOL			20	dB	
Transmitter Reflectance	R_T			-12	dB	
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				2
Average Launch Power OFF	Poff			-30	dBm	
Receiver						
Damage Threshold, each Lane	TH_d	5.5			dBm	3
Total Average Receive				10.5	dBm	
Average Receive Power, each Lane		-10.6		4.5	dBm	
Receive Power (OMA), each Lane				4.5	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-7.7	dBm	
Stressed Receiver Sensitivity (OMA), each Lane				-6.8	dBm	4
Difference in Receive Power between any Two Lanes (OMA)	Prx,diff			5.5	dB	
LOS Assert	LOSA		-18		dBm	
LOS Deassert	LOSD		-15		dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane	Fc			31	GHz	
Conditions of Stress Receiver Sensitivity Test (Note 5)						
Vertical Eye Closure Penalty, each Lane			1.8		dB	5
Stressed Eye J2 Jitter, each Lane			0.3		UI	
Stressed Eye J9 Jitter, each Lane			0.47		UI	

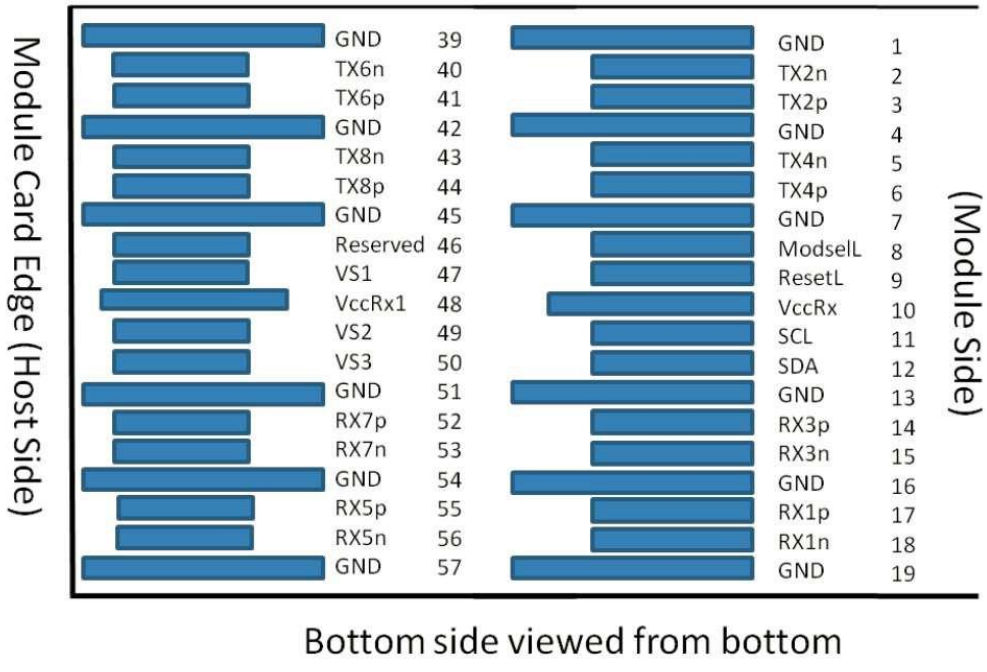
Note：

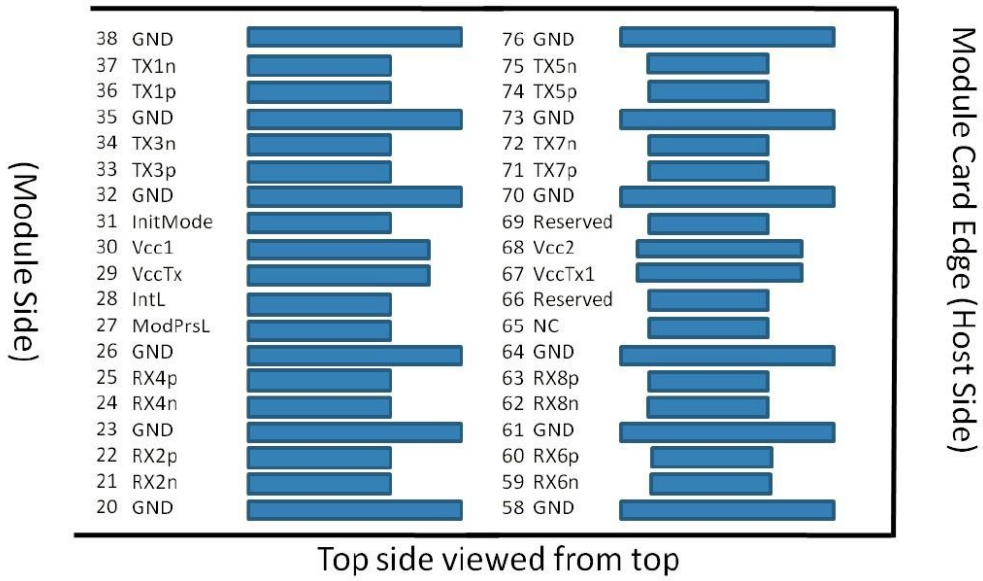
1. Even if the TDP < 1 dB, the OMA min must exceed the minimum value specified here.

2. See Figure below.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Measured with conformance test signal at receiver input for BER = 1x10-12.
5. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



Pin Definitions





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Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS -I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVCMOS -I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

ModSelL Pin

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 13) initiates a complete module reset, returning all user module settings to their default state.

LPMode Pin

LPMode is an input signal. The LPMode signal shall be pulled up to Vcc in the QSFP-DD module (see Table 2). LPMode is used in the control of the module power mode.

See CMIS Section 6.3.1.3.

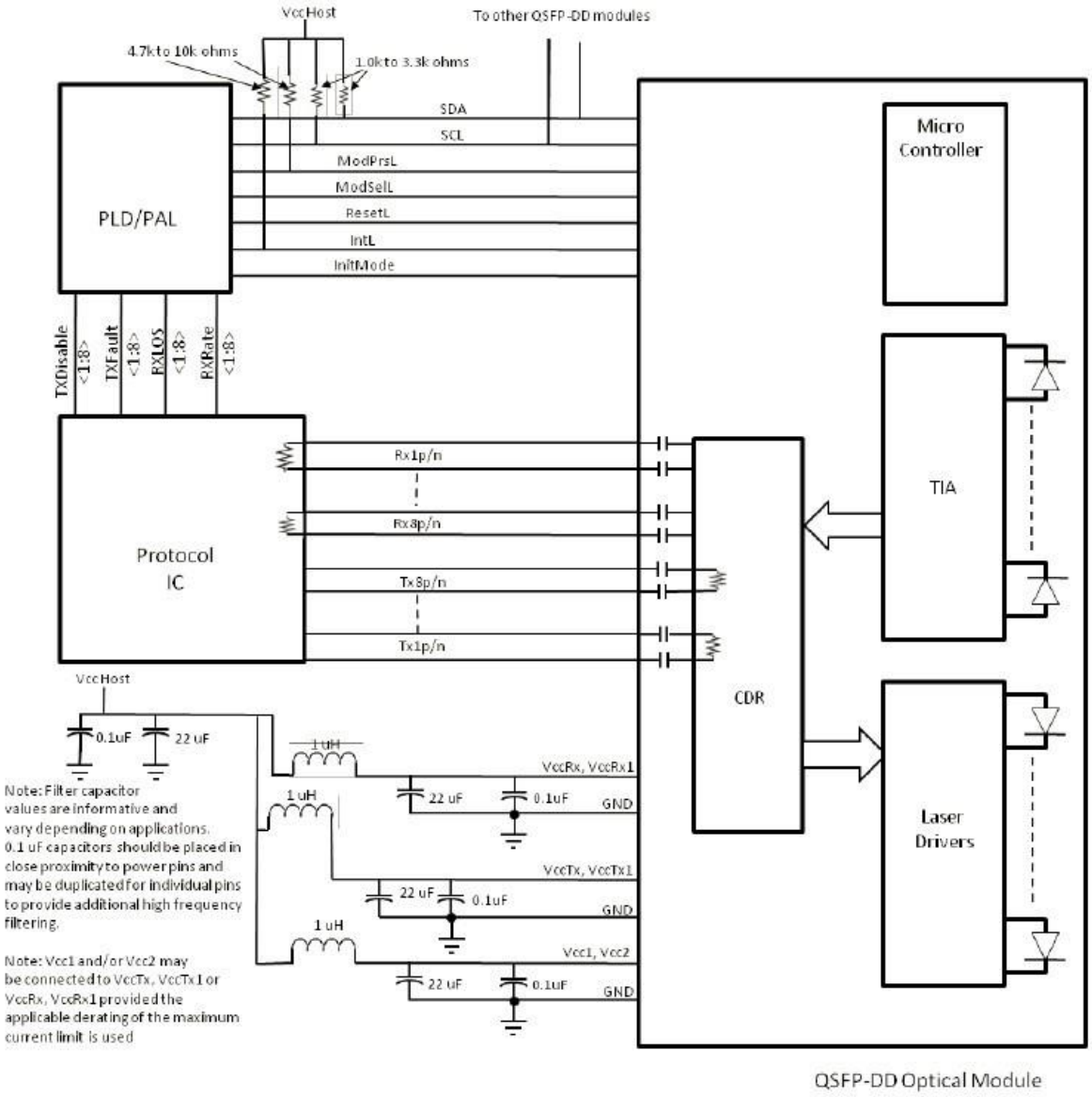
ModPrsL Pin

ModPrsL must be pulled up to Vcc Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

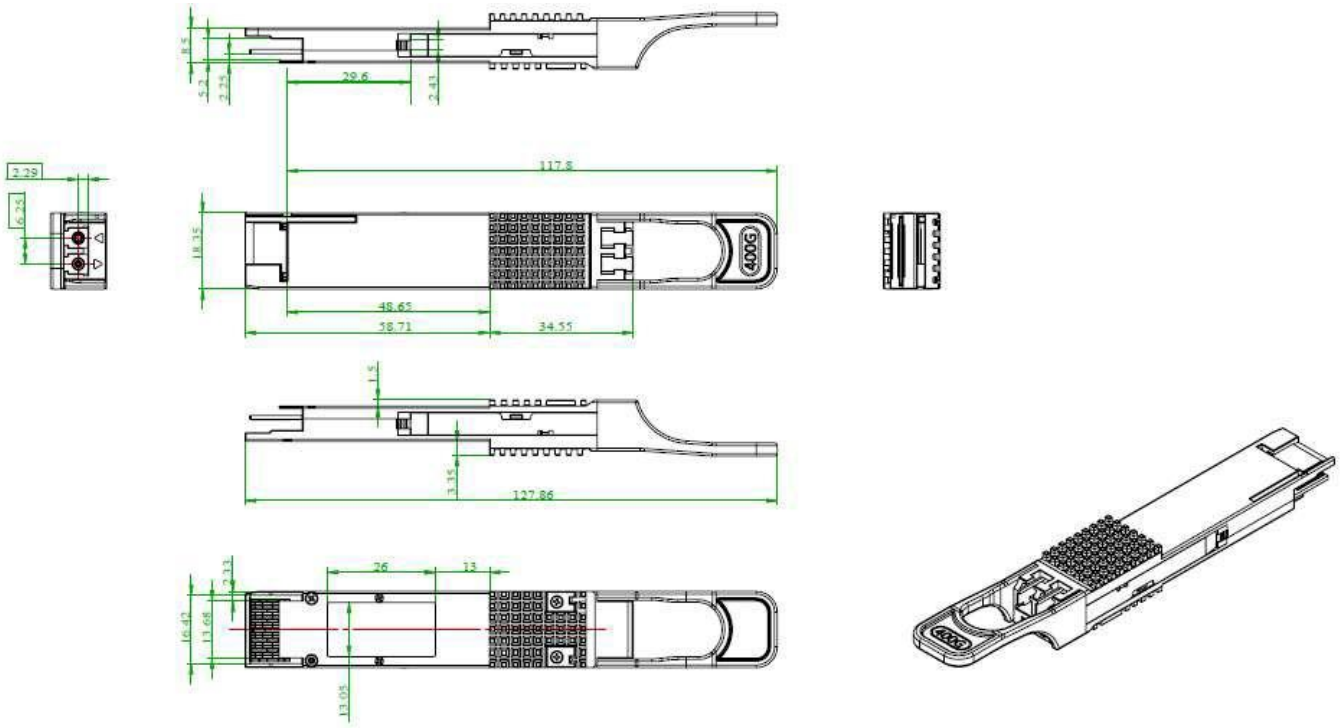
IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted "High" after all set interrupt flags are read.

Recommended QSFP-DD Host Board Schematic



QSFP-DD Host Board Schematic

Mechanical Diagram



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