degree cable shield termination
- ✧ Advantage dual side pre-solder automated assembly technologies
- ✧ Low loss, stronger mechanical features, more flexible
- ✧ QSFP56 modules will be backwards compatible, allowing them to support existing QSFP modules and provide flexibility for end users and system designers

Features:

- ✧ Compliant with QSFP56 MSA Specification Rev 3.4
- ✧ SFF-8679 electrical interface compliant
- ✧ SFF-8636 management interface support
- ✧ Support 50G (PAM4) electrical data rates/channel
- ✧ I2C for EEPROM communication Pull to Release latch design
- ✧ Excellent EMI/EMC performance 360

Applications:

- ✧ Data center & Networking Equipment
- ✧ Servers/Storage Devices
- ✧ High Performance Computing (HPC)
- ✧ Switches/Routers

Standards Compliance

- ✧ IEEE802.3Bj,By,IEEE802.3CD
- ✧ RoHS Complia

● Ordering information

Part Number	SPEED	Specifications		Categories
		Length(mm)	Gauge(awg)	
OPQHT0.5-4	200G	0.5	30	QSFP56 TO 4SFP56
OPQHT1-4	200G	1	30	
OPQHT2-4	200G	2	26	
OPDJT3-4	200G	3	26	

● Product Description:

In an effort to keep up with the demands of higher performance and increasing amounts of memory bus bandwidth, OPWAYdesigners are working to revise, extend and update the solution. OPWAY 200G QSFP56 passive cable assembly can provide new generation performance of QSFP by higher date transfer rate. At the same time, OPWAY QSFP56 TO 4SFP56 cable choose dual side drain cable and self-designed PCBA, provide low loss， less skew and better NEXT. 360 degree EMI crimping shielding and Zinc Die-cast shell designing make the product high-performance. And all

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the designing is based on the industry standard specifications, such as SFF-8679, SFF-8636 and QSFP56 TO 4SFP56 MSA specification rev 4.0.

● Schematic:

QSFP56 TO 4SFP56

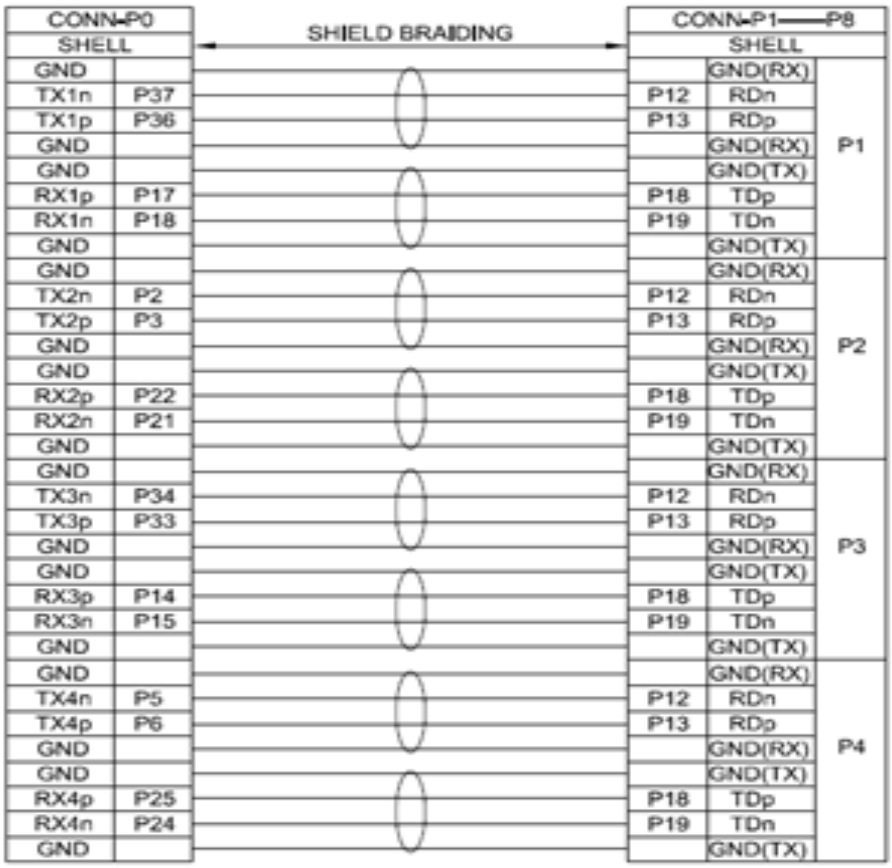


Figure 1 wiring table

● Cable Assembly Characteristics

QSFP56 TO 4SFP56

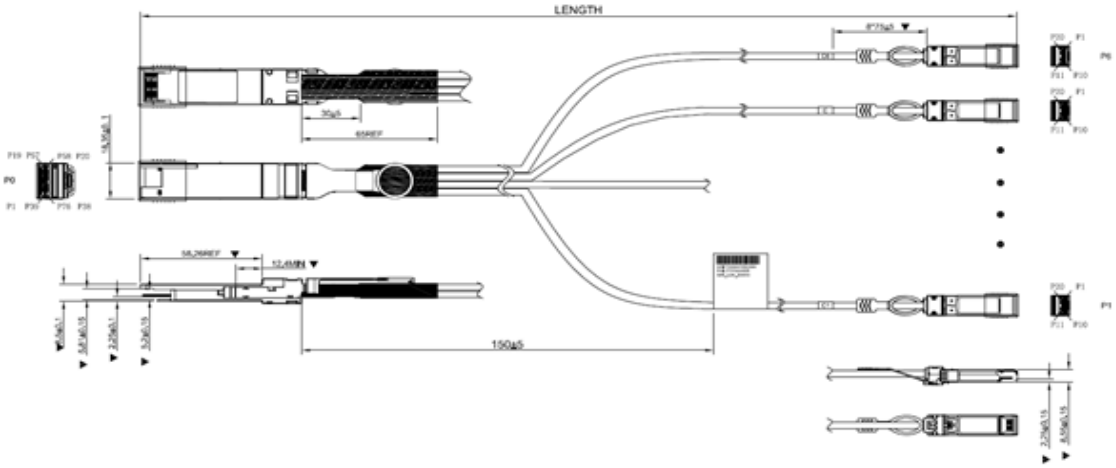


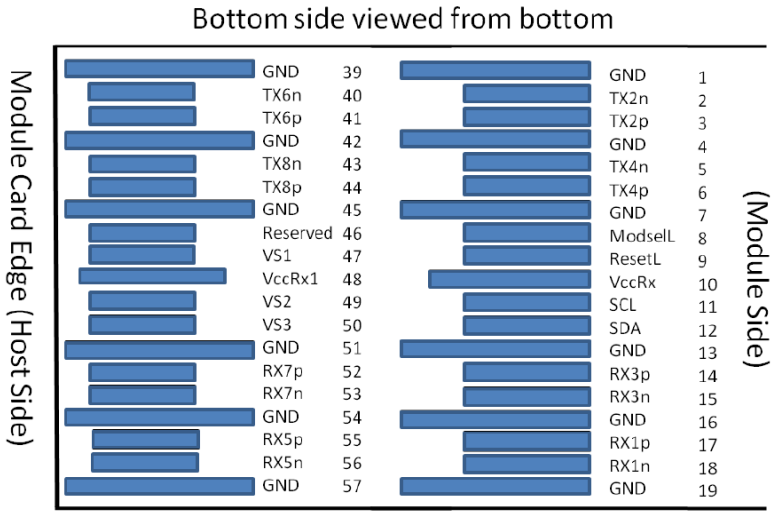
Figure 2 QSFP56 TO 4SFP56 Mechanical Structure

Mechanical Structure Characteristics Of Plug

- ✧ Raw Cable -- Support 26~30AWG, 100ohm, Silver plated, vw-1, RoHS2.0.
- ✧ PCB –High Speed Very low loss material M6,8 Layers Design; Gold finger plated gold 30u" min., nickel plated 150~700u"; pad: immersion gold 1u" min., nickel plated 100u"min. 94v-0, RoHS2.0;
- ✧ Upper shell -- Zinc Die-cast, with Cu plated 280u” min. overall and Ni plated 120u” min.
- ✧ Bottom shell -- Zinc Die-cast, with Cu plated 280u” min. overall and Ni plated 120u” min.
- ✧ Latch-- Stainless steel ,SUS304 + PA66 CM3004,black;
- ✧ Spring -- Stainless steel ,SUS301EH;
- ✧ Rivet -- Stainless Steel, SUS304;
- ✧ SR (Strain Relief) -- PVC, 45P, BLACK, RoHS2.0.
- ✧ Dust Cover—PVC, 60P, Blue, ANTI-STATIC, RoHS2.0.

● Electrical Design

The electrical design of the QSFP56 TO 4SFP56 cable assembly is fully compliant to QSFP56 TO 4SFP56 Hardware Rev4.0 specifications. The electrical design included: a low loss design printed circuit board, DC block capacitances in the Rx channel, and EEprom chips for the management. Pin layout and function definition are shown in Figure 3 and Table 2.



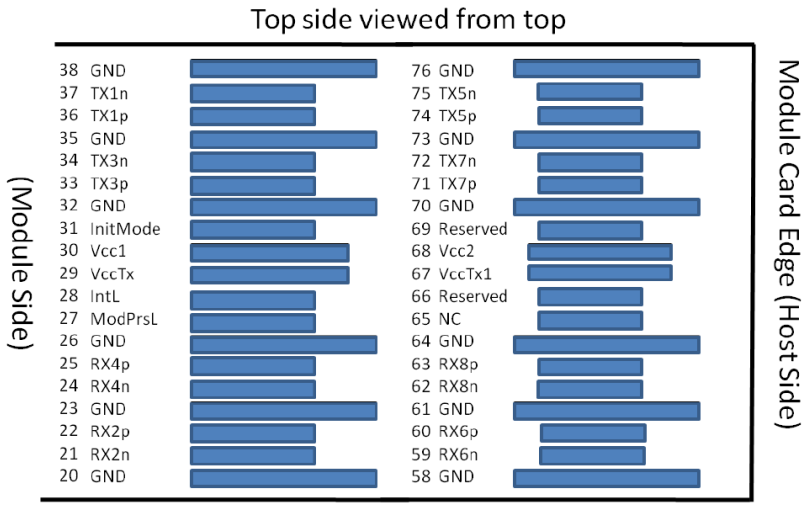


Figure 3 QSFP56 TO 2 QSFP Pin Define

Table2 QSFP56 TO 4SFP56 Pin Function Definition

Pin	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vccl	+3.3V Power Supply	2

31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VSl	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	For future use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	

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76		GND	Ground	1
Note 1: QSFP56 TO 2 QSFP uses common ground (GND)for all signals and supply (power). All are common within the QSFP56 TO 2 QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.				
Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.				
Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.				
Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP56 TO 2 QSFP pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.				

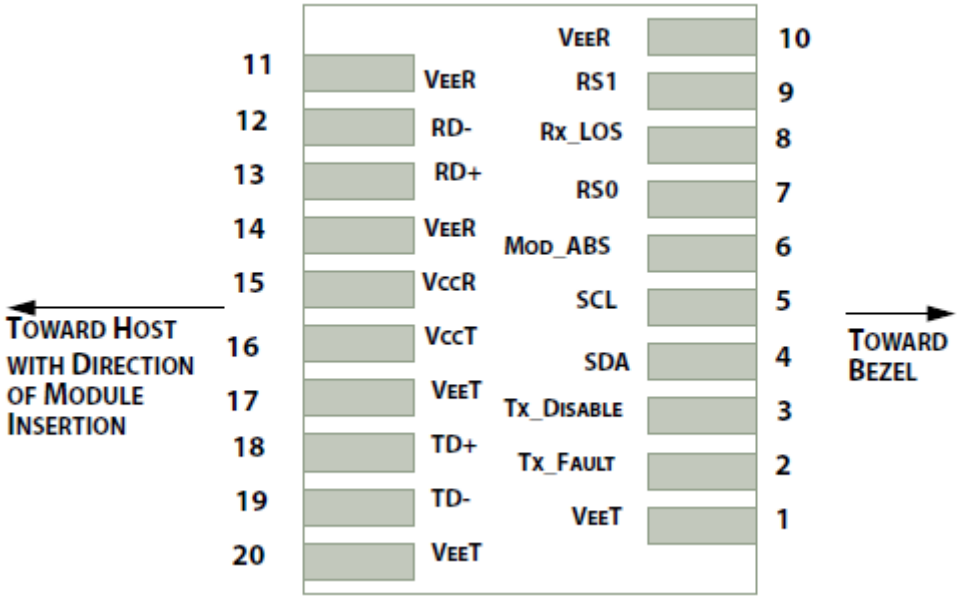
● SFP56 Pin Descriptions

Pin	Logic	Symbol	Name/Description	Notes
1		VeeT	Transmitter Ground	
2	LV-TTL-O	TX_Fault	N/A	1
3	LV-TTL-I	TX_DIS	Transmitter Disable	2
4	LV-TTL-I/O	SDA	Tow Wire Serial Data	
5	LV-TTL-I	SCL	Tow Wire Serial	
6		MOD_DEF0	Module present,	
7	LV-TTL-I	RS0	N/A	1
8	LV-TTL-O	LOS	LOS of Signal	2
9	LV-TTL-I	RS1	N/A	1
10		VeeR	Reciever Ground	
11		VeeR	Reciever Ground	
12	CML-O	RD-	Reciever Data Inverted	
13	CML-O	RD+	Reciever Data	
14		VeeR	Reciever Ground	
15		VccR	Reciever Supply 3.3V	
16		VccT	Transmitter Supply	
17		VeeT	Transmitter Ground	
18	CML-I	TD+	Transmitter Data	
19	CML_I	TD-	Transmitter Data	
20		VeeT	Transmitter Ground	

Notes：

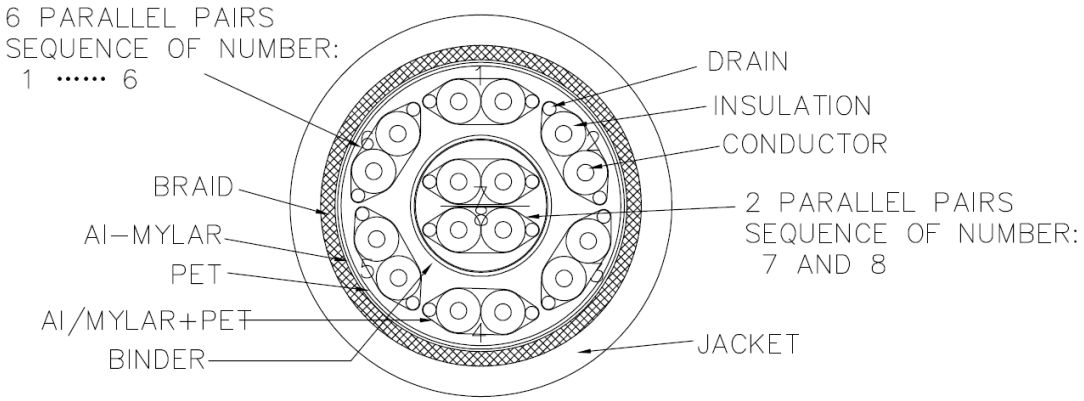
1. Signals not supported in SFP56 Copper pulled-downto VeeT with 30K ohms resistor
2. Passive cable assemblies do not support LOS and TX_DIS

● Host PCB SFP56 pad contact assignment



● Bulk Cable Characteristics

The structure of the cable is shown as the figure , the characteristics of the bulk cable are listed below.



SECTIONAL DRAWING:

- ✧ Voltage rating: 30V
- ✧ Temperature rating: 80℃;
- ✧ Impedance: Differential mode: 100 +5/-5 ohm @TDR;
- ✧ Delay Skew(INTRA-SKEW): 30ps/5m max;
- ✧ Signal Twin-ax pair cable: Solid Ag plated copper conductor;
- ✧ Braid shielding coverage 85% min.
- ✧ Jacket material: PVC

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